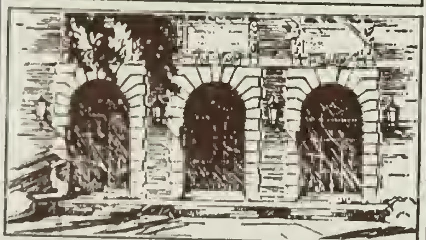

Report No. 191

# SOME INVESTIGATIONS IN THE AREA OF HIGH VOLTAGE, HIGH CURRENT D-C AMPLIFIERS

by

Marlin Everett Greer



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DEPARTMENT OF COMPUTER SCIENCE · UNIVERSITY OF ILLINOIS · URBANA, ILLINOIS

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# SOME INVESTIGATIONS IN THE AREA OF HIGH VOLTAGE, HIGH CURRENT D-C AMPLIFIERS*

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Department of Computer Science
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* This work was submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering, August, 1965.

## ACKNOWLEDGMENTS

The author would like to express his gratitude to Professor K. C. Smith for his inspiration and guidance in this project.

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# INTRODUCTION

A d-c amplifier, to be truly versatile, must satisfy a diversity of normally conflicting requirements. It must be, for example, tolerant of both large and small loadings, and to be capable of large output swings, at least for small loads.

Available devices incorporating solid-state circuitry normally have a very limited range, being either high voltage, low current, or high current, low voltage amplifiers. In fact, it appears that the present state of the art, as far as marketable fairly-high-speed amplifiers[1] is concerned, provides up to $\pm$ 20 volt swings and load current limits of 0.5 amp with some specialized amplifiers extending one of these parameters at the expense of the other.

The intent of this paper is to investigate the feasibility of extending the ranges of both output parameters considerably; and, at least, in some special way make available both high voltage and high current output capability in the same amplifier. Problems involved in this area will be investigated. A search will be made for promising circuit designs.

It is anticipated at the beginning that the time will not necessarily permit a complete solution to the problem stated in the following pages; but, rather the intent is to devise possible areas of attack and to explore the feasibility of designs suggested from these possibly different points of view.

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[1]Excluded are the class of slow d-c amplifiers which are available as reconnections of modern versatile regulated power supplies.

## 1. AVAILABLE TRANSISTORS

High current transistors have been available for some time, though the technology for high voltage transistors has been slower in developing; however, devices are now available rated up to 600 volts (maximum collector to emitter voltage). An example of a moderately priced NPN device is the Industro Corporation, TRS3605S, with the following specifications:

Absolute Maximum Ratings

| | |
|---|---|
| Collector to emmiter voltage | 420 volts |
| Collector to base voltage | 420 volts |
| Emitter to base voltage | 5 volts |
| Collector Current | 400 ma. |
| Total dissipation @ 25 C Ambient | 2 watts |

Typical Values

| | |
|---|---|
| $H_{FE}$ at 10 ma. | 30 |
| $H_{FE}$ at 200 ma. | 25 |

Both PNP and NPN high current transistors are available. However, high voltage transistors are at present limited to NPN polarity. A further difficulty is that both high voltage and high current transistors have rather poor gain.

The possible combined use of high voltage transistors to extend the maximum output voltage ratings and high current transistors to extend the maximum output current ratings will be investigated. It is intended by this means to produce an amplifier which, though limited in total power drive capability, is versatile by being able to provide both relatively high voltage output into high resistance loads, and relatively high current output into low resistance loads. One possible output characteristic of such an amplifier is shown idealized in Figure 1.

Incidentally, to be very useful, the desired amplifier configuration should not compromise bandwidth, linearity, or any of the other criteria of standard amplifier merit.

The design problem seems to lend itself to separation into two parts: A preamplifier using more common low power, low voltage transistors, and a high power, high voltage stage.

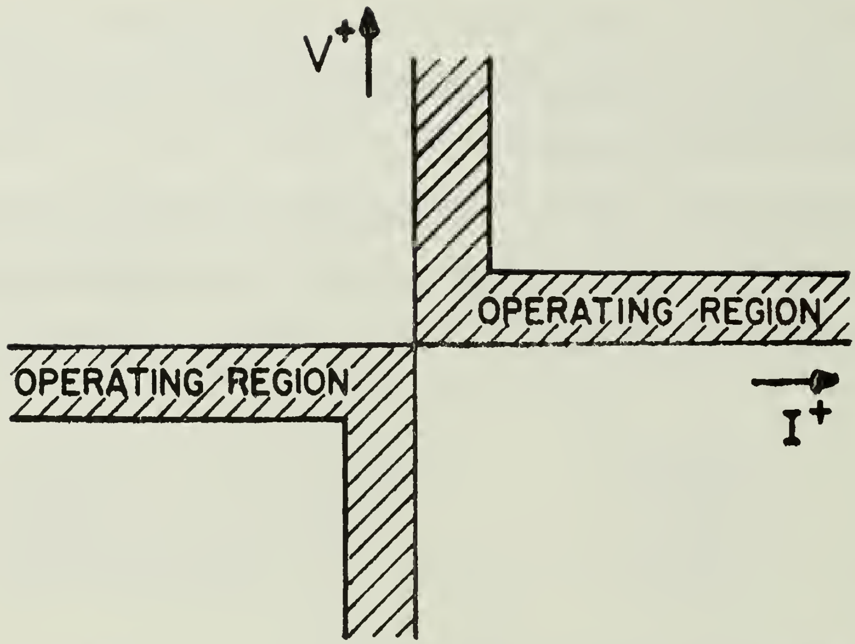


FIGURE I. IDEALIZED OUTPUT CHARACTERISTICS OF AN AMPLIFIER STAGE WITH GROUNDED LOAD.

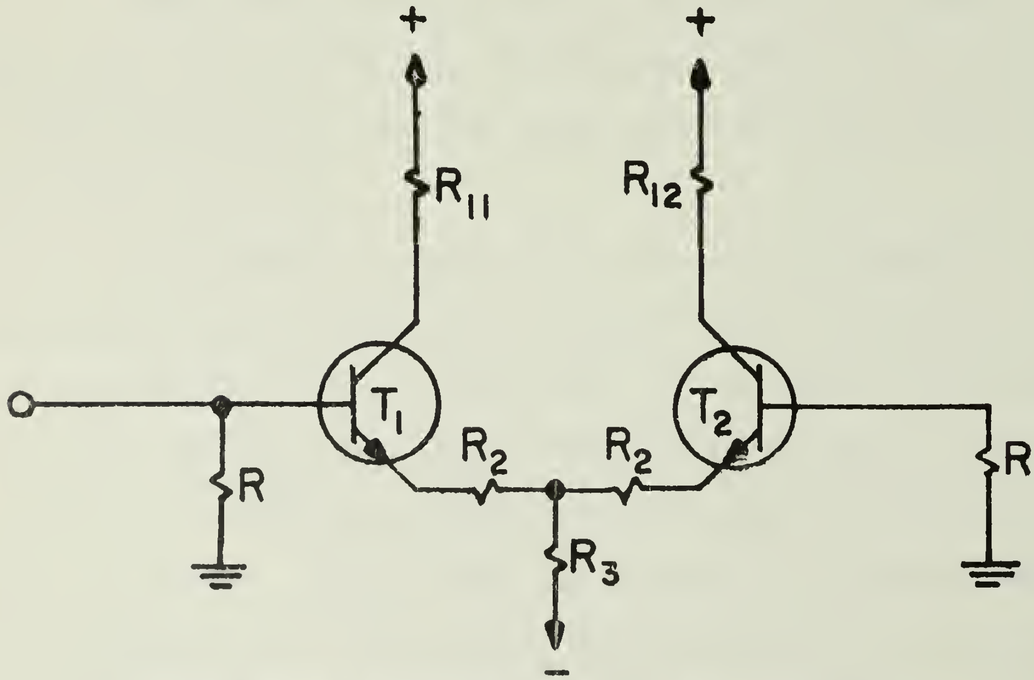


FIGURE 2. A DIFFERENTIAL AMPLIFIER STAGE.

## 2. THE PREAMPLIFIER

For one possible intended use of the completed unit, as an operational amplifier, the preamplifier will need high d-c gain of perhaps several thousand. Because of its d-c gain and d-c coupling, this stage will tend to be unstable. It will, for example, tend to drift due to changes in leakage current in the transistors caused by temperature changes.

Accordingly, a decision was made to use a differential amplifier as the standard building block because of its inherent stability against such drift.

Figure 2 is an example of such an amplifier. The two transistors ideally would be identical to each other or closely matched in a variety of parameters and their thermal coefficients. The two transistors should also be physically and electrically close to each other, located in a thermal and electrical enclosure such that the environment of each is identical.

The latter precautions are to ensure that the transistors will be subjected to the same temperature so that they will have identical leakage current, base to emitter voltage, and current gain changes.

Identical leakage current changes will affect the circuit in the same manner as does a common mode (CM) signal. A CM signal is one in which signals of the same phase and magnitude are applied to the bases of both transistors.

A differential mode (DM) signal is represented by a signal to the base of one transistor and a signal of the opposite phase but same magnitude to the other base.

It is important to notice that a differential amplifier has a CM and a DM gain which are different. The CM gain needs to be made as low as possible in order to enhance the stability of the circuit against drift.

There is also another important reason to do this. For preamplifier use, only one signal is normally available. Therefore, no corresponding out of phase signal will be applied to the corresponding base of the other transistor. This one-sided signal is in effect a combination of a CM and a DM signal. A differential mode signal of two volts, for example, would consist of a positive one volt signal on the left base and a negative one volt signal on the right base.

Note that a positive one volt signal on the left with no corresponding signal on the right is in effect a DM signal of one-half volt raised by a CM signal of one-half volt. This occurs because the signal divides across the two emitter resistors or their equivalent.

If the CM gain is large, therefore, this common mode signal would cause an equal but undesirable change in the two collector voltages. If, for example, the output is considered to be taken from one side of the amplifier only, the resulting CM output is indistinguishable from an amplified DM signal.

To demonstrate a means of overcoming this problem, the circuit will be investigated in more detail.

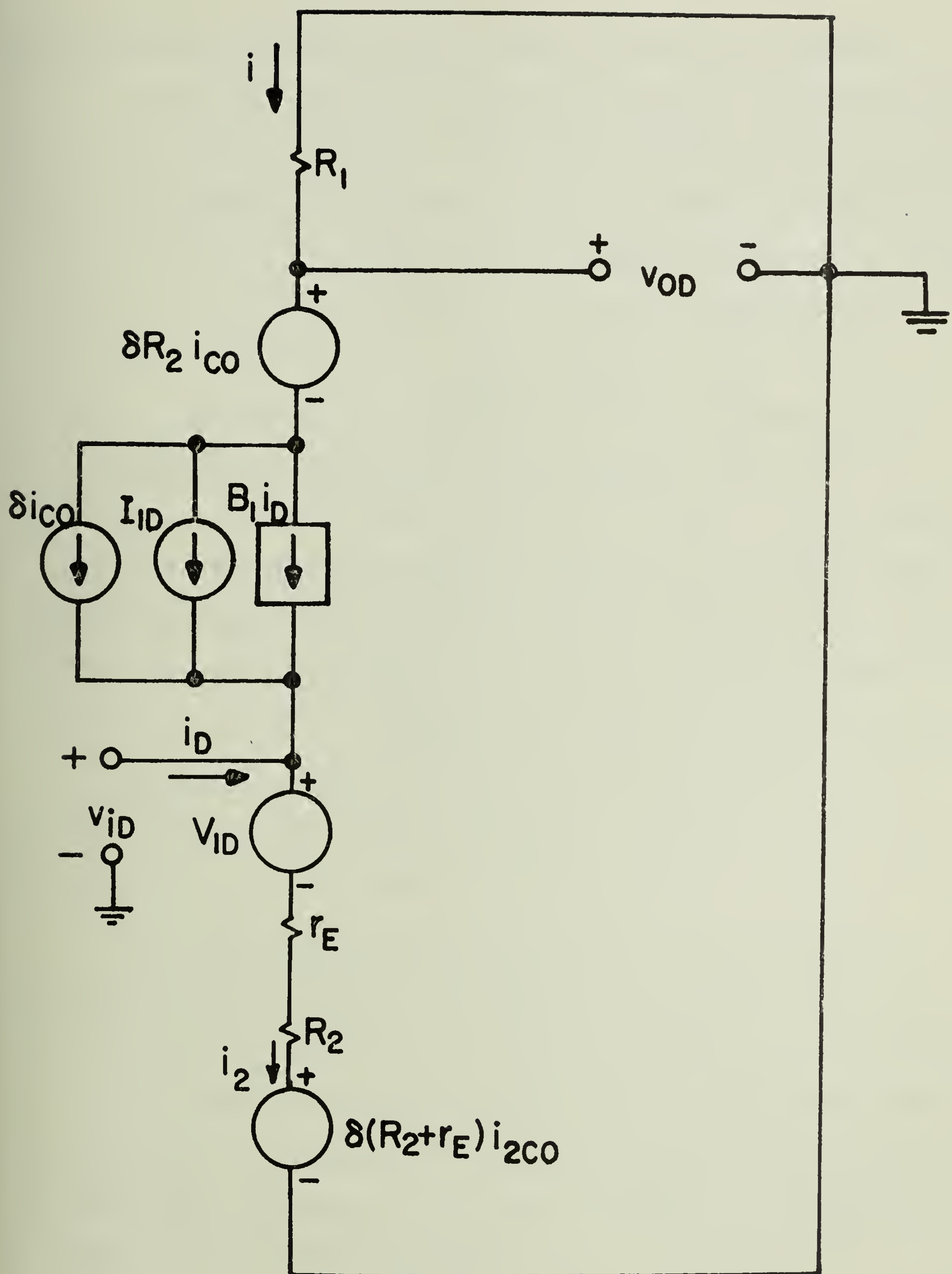


FIGURE 3. DIFFERENTIAL MODE EQUIVALENT HALF CIRCUIT FOR AN UNBALANCED DIFFERENTIAL AMPLIFIER.

Consider the circuit in Figure 3 as an equivalent half-circuit for the differential amplifier in the differential mode. The square represents the usual controlled generator of a transistor model. The circle generators represent uncontrolled generators. The symbol $\delta$ is a measure of the degree of unbalance in the circuit.

The following parameters are defined:

$$V_{1D} = \frac{V_{BE1} - V_{BE2}}{2}$$

$$I_{1D} = \frac{I_{CO1} - I_{CO2}}{2}$$

The letter "D" subscript indicates states due to differential mode effects and the letter "C" (to appear later) to common mode effects. The symbols $V_{BE1}$ and $V_{BE2}$ are the base to emitter voltage drops of transistor, $T_1$ and $T_2$ respectively and $I_{CO1}$ and $I_{CO2}$, are their leakage currents.

The $\delta$ generators represent current and voltage changes in the circuit due to the CM part of the signal voltage.

where:

$$V_{IC} = \frac{V_{BE1} + V_{BE2}}{2}$$

$$I_{IC} = \frac{I_{CO1} + I_{CO2}}{2}$$

$v_{IC}$ is the common mode signal and $v_{ID}$ is the differential mode signal. The differential mode voltage at the output ($v_{OD}$) is then:

$$v_{OD} = -\delta R_1 i_{1CO} - \frac{\alpha_1 R_1}{R_2 + r_E}\left[v_{ID} - V_{ID} - \delta(R_2 + r_E) i_{2CO}\right] - R_1(I_{1D} + \delta\beta_1 i_{CC})$$

Therefore, to make the circuit a true DM amplifier we need to nullify the effects of the common mode currents (suffixed with the letter "c").

The immediately obvious way to do this is (by looking at the expressions for the CM currents) to make $R_3$ arbitrarily large; however, to do this directly is to reduce the current capabilities of the amplifier.

At a fixed current level, $R_3$ must act as a current source; therefore, if $R_3$ were to be exchanged for an ideal current source, the amplifier would see infinite impedance at this point. A solution to the problem is to replace $R_3$ by the circuit in Figure 4.

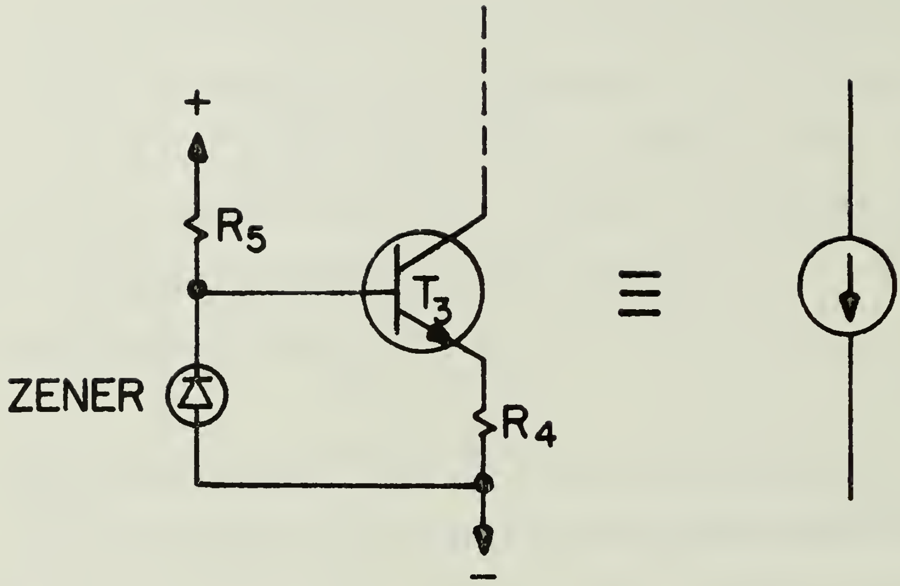


FIGURE 4. CONSTANT CURRENT GENERATOR.

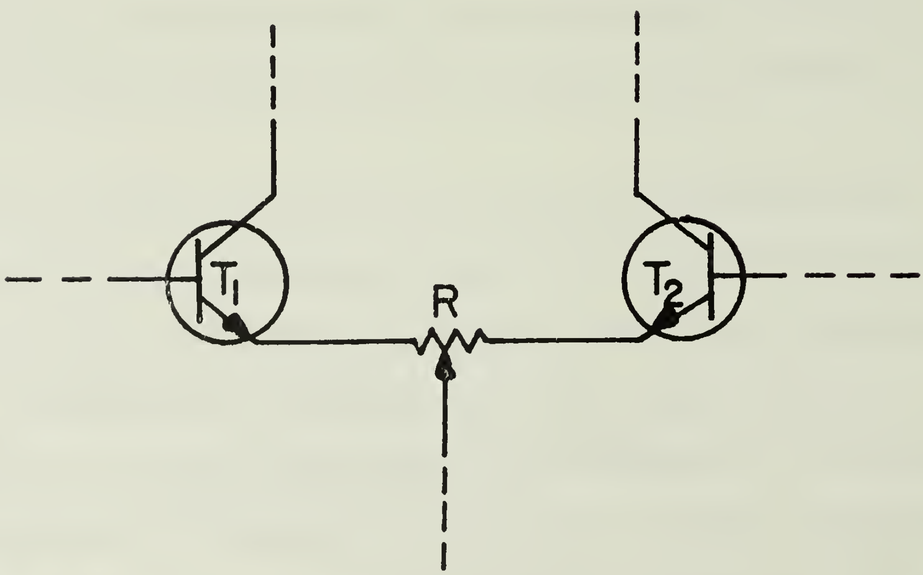


FIGURE 5. CIRCUIT FOR BALANCING THE DIFFERENCE OF BASE TO EMITTER DROPS.

In this current generator the zener diode controls the voltage drop across $R_4$ and with appropriate values of zener voltage and resistance for $R_4$, any desired current can be obtained. Appropriate choice of zener temperature coefficient will compensate over a meaningful range for variation of emitter-base voltage drop and other parameters of $T_3$.

The differential amplifier now sees $r_c$ of the transistor which is the order of several megohms.

The equation for $v_{OD}$ has now been effectively reduced to:

$$v_{OD} = -\alpha_1 R_1 \frac{v_{ID} - V_{1D}}{R_2 + r_E} - R_1 I_{1D}$$

$I_{1D}$ can be made reasonably small by carefully choosing the two transistors to be well matched. This matching process also helps lower $V_{1D}$--the difference in base to emitter drops of the two transistors. These differences can be further reduced by using a balance resistor as in Figure 5.

The differential mode gain can now be approximated as:

$$A \approx \frac{\alpha R_1}{R_2 + r_E}$$

where $r_E$ includes the appropriate part of the balance resistor.

However, as was discussed earlier, the gain will be reduced by a factor of two when used as an unbalanced-input preamplifier. This is due to the fact that the corresponding out of phase signal will not

be applied to the opposite base.[2]

The ideas redeveloped in this section will be used in the next chapter to build and test an actual preamplifier with a high voltage output stage.

[2]For a more complete discussion of d-c amplifiers, see R. D. Middlebrook, Differential Amplifiers (John Wiley and Sons, Inc., New York), 1963.

## 3. A HIGH VOLTAGE AMPLIFIER

The circuit in Figure 6 is capable of driving small loads with large voltage swings. By virtue of high impedances its response will be somewhat slow. The differential stage on the left is the preamplifier. The resistor to ground on the collector of $T_1$ is to balance the effect of the voltage divider on the collector of $T_2$. The purpose of the voltage divider to the negative 350 volt supply is to translate the available signal toward ground permitting the base of $T_3$ to be negative with respect to the collector in order to permit negative swings.

The gain of the circuit is about:

$$A = \frac{1}{2} \frac{\alpha R_1 // R_2}{R_B/2 + r_E} \approx 1000$$

which checked closely experimentally.

The output stage, including the adapting voltage divider, has a small gain of about three, allowing the preamplifier to be used with slightly smaller swings.

The circuit will handle output swings of up to $\pm$ 200 volts for small loads of the order of one megohm.

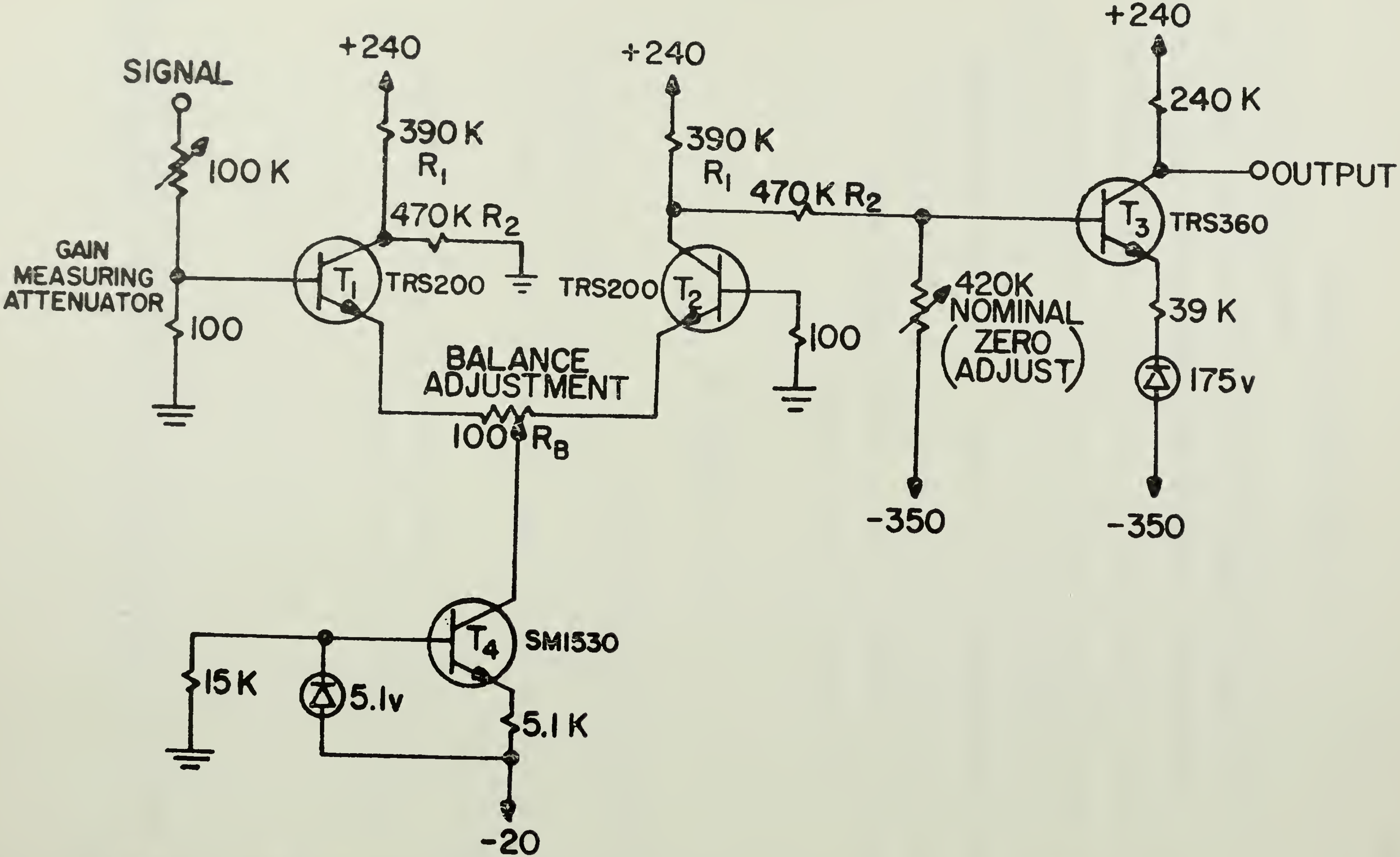


FIGURE 6. HIGH VOLTAGE OUTPUT STAGE DRIVEN BY A DIFFERENTIAL PREAMPLIFIER.

## 4. INCREASING DRIVE CAPABILITIES

Circuits of the type exemplified by the output stage of the previous high voltage amplifier must be abandoned, because of their inherent ineffectiveness in the use of the current and power ratings of the output transistor. This combined-transistor resistor design forces several times the maximum available current for one polarity of output swing to exist as additional useless load on the transistor for the other output polarity.

In an attempt to allow the circuit to handle low resistance load, the concept introduced earlier (Figure 1) of supplying the necessary current for low resistance within a restricted output voltage range, is incorporated in the circuit to follow.

The circuit in Figure 7 is noted to look promising. It would be conceived of as a high power output stage driven by a preamplifier. For $R_L$ large, current drain will be small, leaving the collector voltages large in magnitude. The diodes will, therefore, keep the low voltage supplies out of the picture. For positive swings only the top transistor will conduct, and conversely, the lower for negative swings.

Large loads will reduce the magnitude of the collector voltages allowing the circuit to reduce to that of Figure 8. The transistors are now not inhibited by collector resistors, allowing the amplifier to drive small resistance values easily over a limited voltage range. Typically, but dependent upon application, the available current would be limited by fuses, resistors, or the inherent characteristics of the power supplies. Although this configuration reduces greatly the problem of high dissipation which occurs if both large voltages and currents are allowed, it does, of course, have the practical limitation that there are no high voltage, high current devices presently in existence. Thus, in an amplifier designed with present

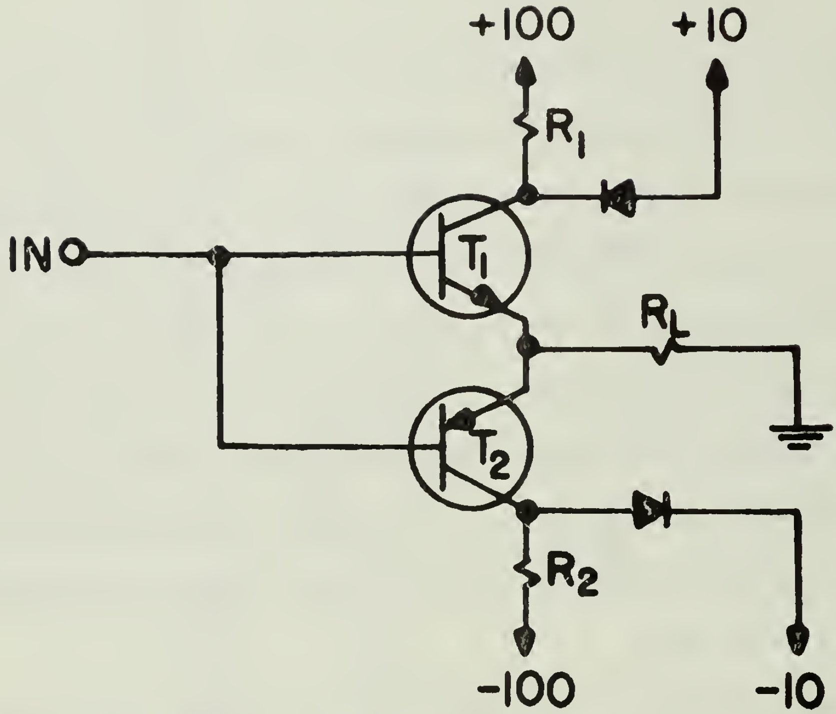


FIGURE 7. HIGH POWER OUTPUT STAGE WITH ALTERNATE HIGH CURRENT OR HIGH VOLTAGE CAPABILITIES APPROXIMATING THE OUTPUT CHARACTERISTICS OF FIGURE 1.

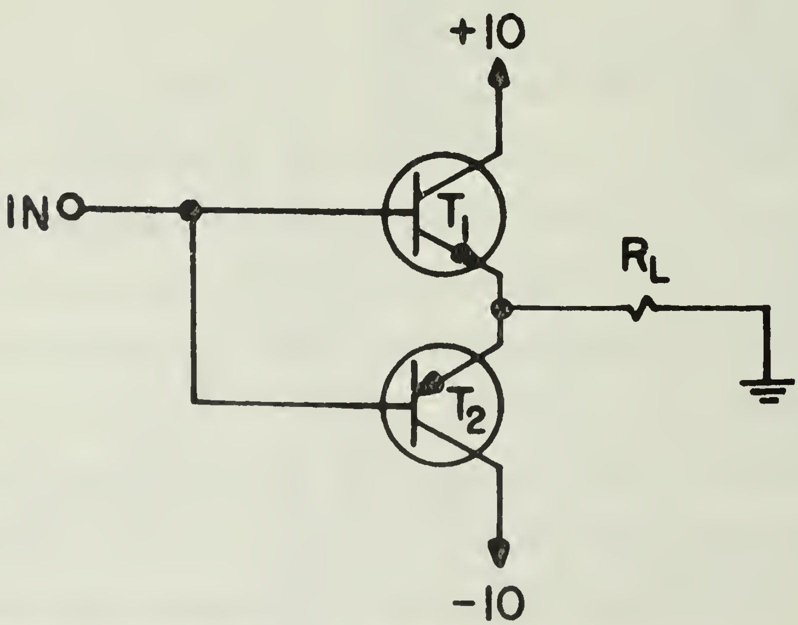


FIGURE 8. HIGH CURRENT OUTPUT EQUIVALENT CIRCUIT.

technology a high current limit would have to be traded for lower voltage capabilities and/or conversely high voltage for low current. A further difficulty is that no really high voltage PNP devices are presently available.

Possible methods of overcoming the problems of this simple approach will be studied in the next section.

# 5. HIGH CURRENT DRIVES

The problems of driving large loads are now explored, ignoring for the moment the difficulties of incorporating large voltage swings.

## 5.1 Complimentary Emitter Circuit

It was noticed earlier that the circuit in Figure 7 has high current drive properties which operating in the mode shown in Figure 8.

A stage of this type provides current drive with no voltage amplification. The load voltage nearly follows the input (with the exception of a lag of 0.5 volts or so depending on $V_{BE}$ of the device).

This stage has the advantage that it draws no standby current and only one transistor is working at a time. For example, with a positive signal, the top transistor drives the load with the bottom transistor acting as a reverse biased diode. It also will handle very large loads before being overcome by collector dissipation since it may have limiting resistors in either the emitter or collector paths.

Despite its very promising first appearance the stage has a very serious problem--it will not amplify small signals. The base-emitter voltage drop creates a nearly "dead" region of twice $V_{BE}$ in magnitude.

This problem gives the stage the output characteristic as shown in Figure 9.

The circuit also has the disadvantage of needing complimentary transistors, which are, however, available in high-current, low-voltage devices.

To overcome the first problem a small standby current may be set up through the two transistors as is shown in Figure 10.

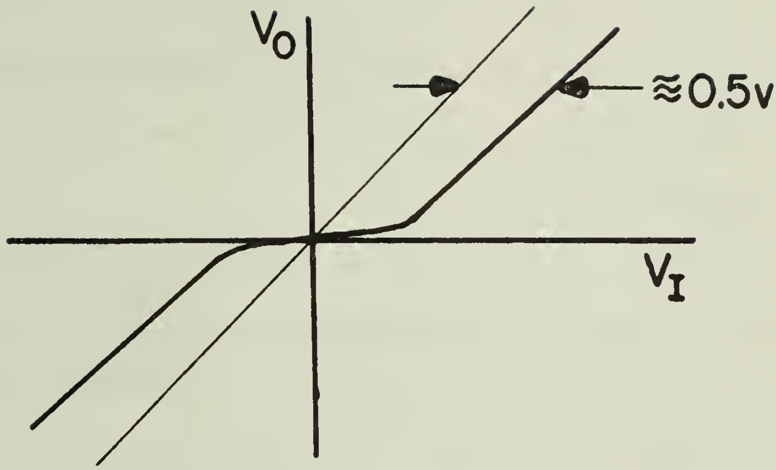


FIGURE 9. OUTPUT CHARACTERISTIC OF A SIMPLE COMPLIMENTARY EMITTER FOLLOWER OUTPUT STAGE.

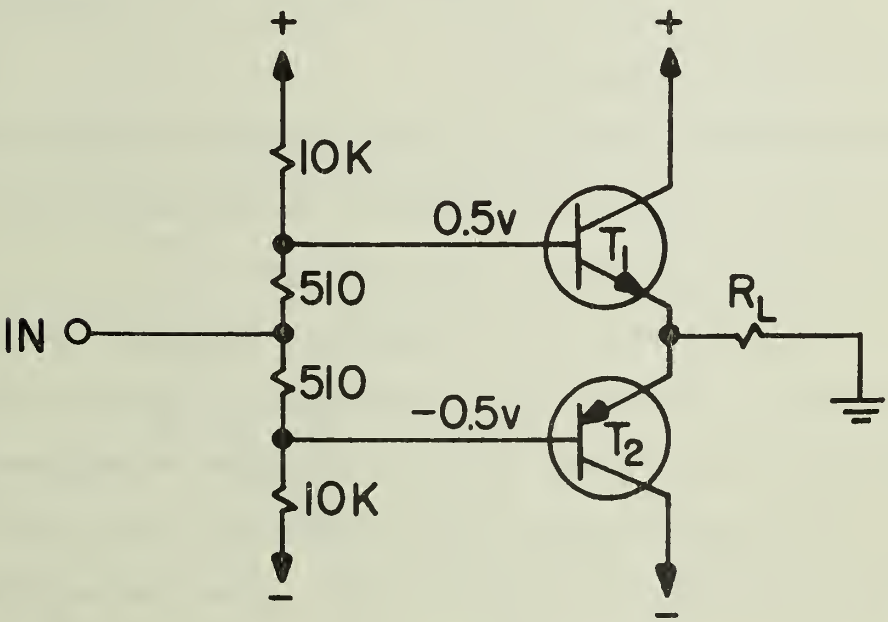


FIGURE 10. BIASING CIRCUIT TO OVERCOME DEAD REGION PROBLEM.

This will allow the drive of small signals as desired, but the solution creates another difficulty--the possibility of a short circuit, or at least an uncontrolled current, through the two transistors from the positive to negative supply.

Experimentally, if the bias resistors are increased to 820 ohms--that is, biasing the base somewhat above the $V_{BE}$ drop required, to ensure that the dead region is completely eliminated--a complete short is not found but a large uncontrolled standing current does result.

It is further verified that once this condition is set up, the application of a signal does not shut off one of the transistors. For instance, for a positive signal, although the base voltage is raised tending to shut off the lower transistor, there is a short circuit path through the two emitters and the emitter will therefore follow the base up leaving the short circuit path still available. The detailed behavior is, of course, load dependent.

An attempt at controlling this short might be made by observing that when the top transistor is conducting, the bottom one should be shutting of and vice versa as is shown in Figure 11.

For example, when $T_2$ is conducting sufficiently that $R_2$ drops enough voltage to allow the control transistor $T_4$ to conduct, base current is drawn away from $T_1$, through the collector of the control transistor $T_4$.

This system when tried in the simple form shown in the figure turned out to oscillate, for no input signal, between three states: $T_1$ on, $T_2$ on, and both $T_1$ and $T_2$ off.

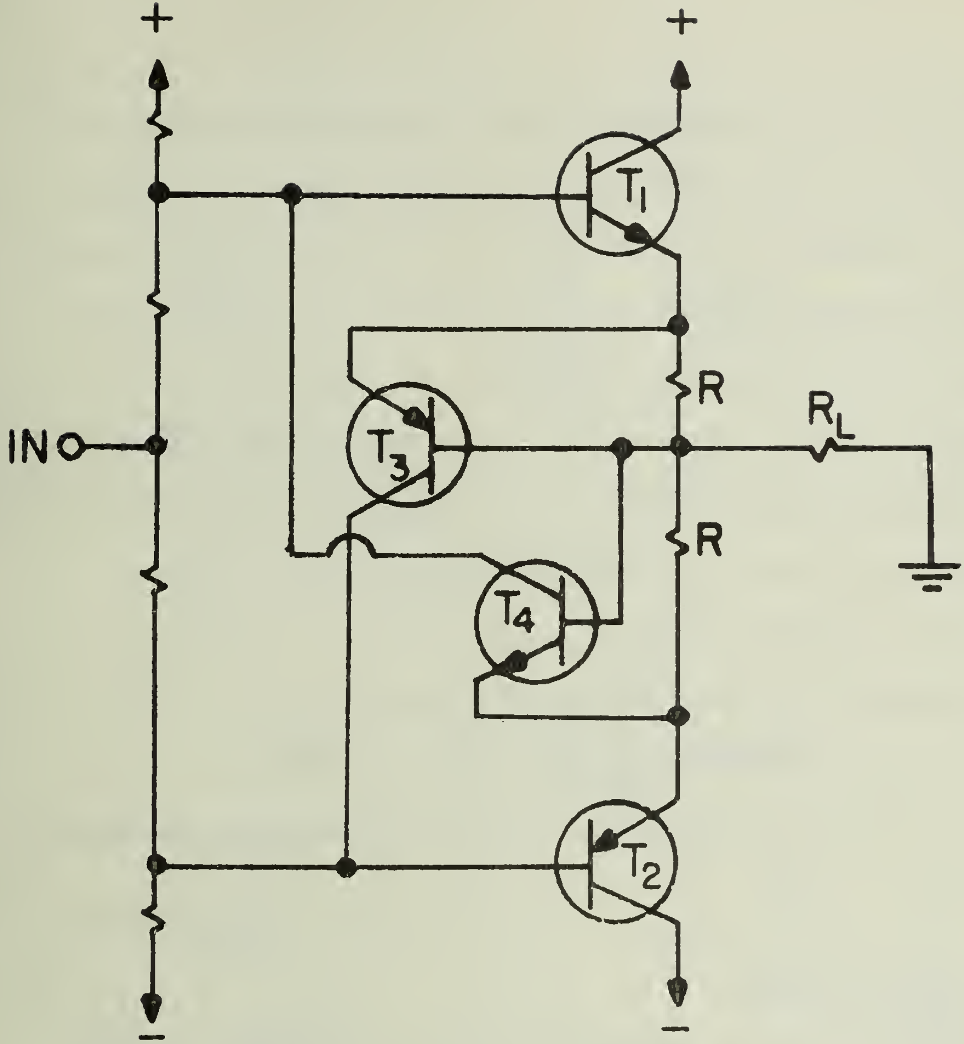


FIGURE 11. HIGH CURRENT DRIVE STAGE WITH SHORT CIRCUIT CONTROL.

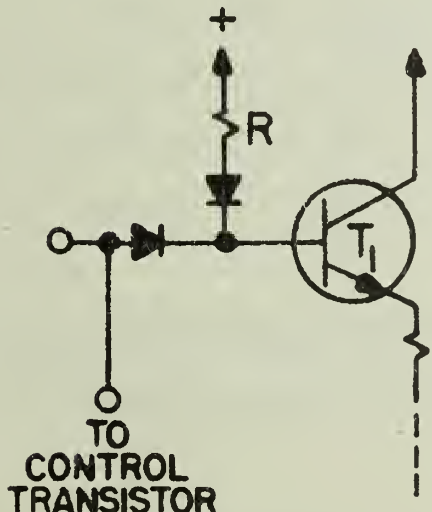


FIGURE 12. BIASING METHOD TO PROVIDE STANDING CURRENT OUT OF REACH OF THE CONTROL TRANSISTOR.

The system can be made more stable by providing $T_1$ and $T_2$ with a minimum current out of reach of the control transistors. This idea is illustrated in Figure 12. R would be large to keep the standby current small. Stability can also be enhanced by reducing loop gain with series emitter resistors in the control transistors.

Though it may be perfected, the system appears not to have surmounted the "dead" region problem.

The control transistor technique attempted above, in fact, only disguises the inevitable problem of this class of circuit--that of change of base-emitter voltage offset with imposed load.

Difficulties experienced in improving the circuit from this point of view led to the development of another configuration which will be described next.

## 5.2 Emitter-Follower Circuit

In the search for a configuration that does not have the inherent problem of base-emitter voltage cutoff with load, consider Figure 13.

The circuit shown operates as a class A type output stage with release of pulldown current during pullup. This property overcomes the problem of changing from negative signals, where $T_2$ is expected to conduct, to positive signals where it is to cut off. This also prevents the possibility of a short through $T_1$ and $T_2$.

Uncontrollable current through $T_1$ and $T_2$ is not a problem in this type of configuration since $T_1$ sees the collector impedance of $T_2$, which acts as a current source.

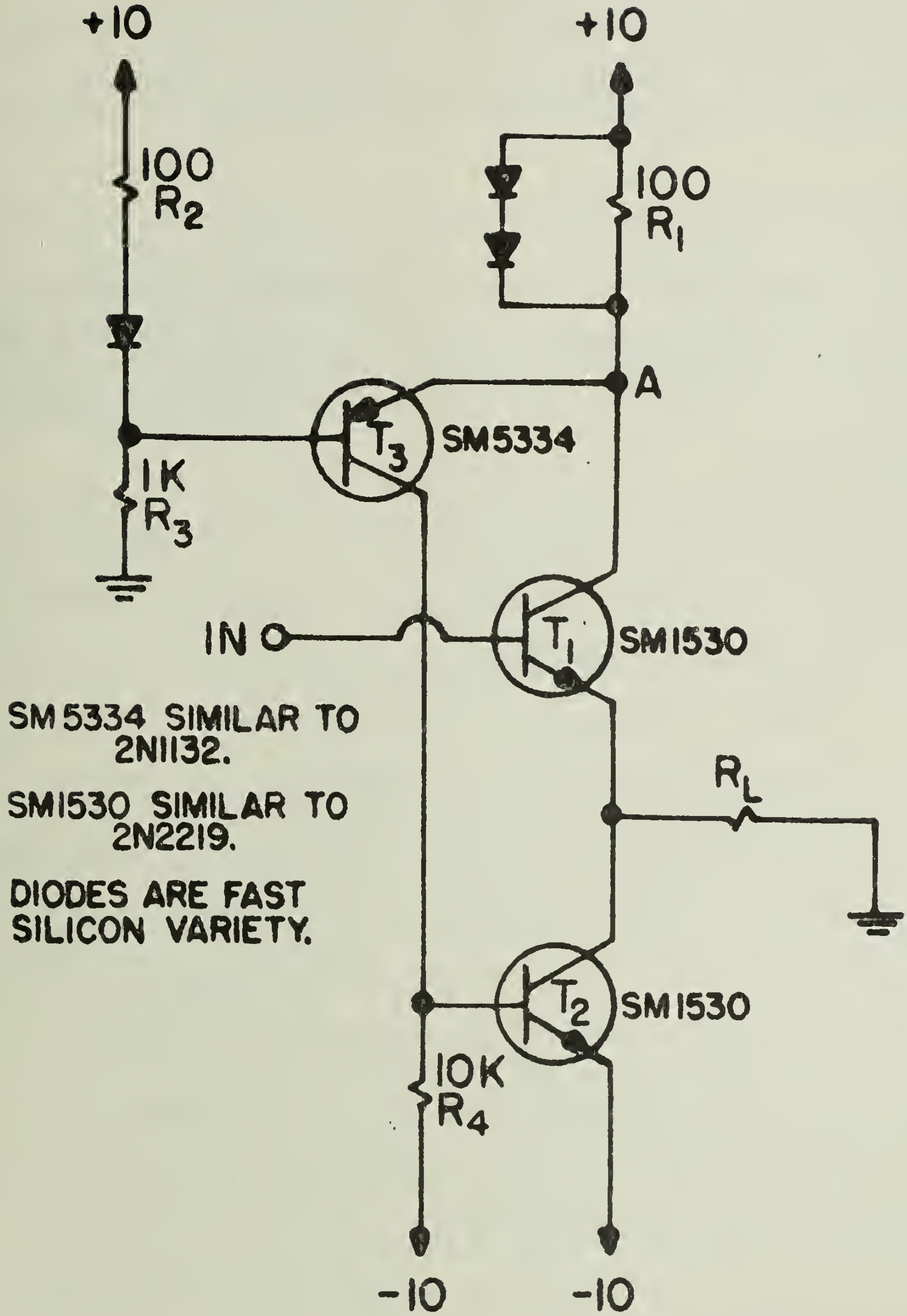


FIGURE 13. EMITTER FOLLOWER HIGH CURRENT OUTPUT STAGE.

Since $T_1$ needs only a small amount of standby current and $T_2$ cuts off for negative drive, the stage has very efficient current drive capability.

The resistor, $R_1$, is present as a drive for $T_3$. But, it is made small so that $T_1$ will not saturate out as load increases. Ideally, $T_3$ should bias $T_2$ off for positive signals, drive the base of $T_2$ for negative signals; and establish a controlled standing current through $T_1$ and $T_2$ for the no signal case.

Positive signals will bias $T_3$ off, turning $T_2$ off and allowing $T_1$ to drive only the load with no loading by $T_2$. For negative signals $T_3$ will be biased on providing base current for $T_2$.

Since $R_1$ tends to saturate $T_1$ at large loads, it is desirable to bypass it, if possible, after its role in turnoff of $T_3$ is complete and before it has this effect on the circuit. For zero input, the voltage drop across $R_1$ is about one volt. It takes very little increase in this drop to completely turn $T_3$ off. If this drop, after reaching one and one-half volts or so could be held at this point with the resistor bypassed, the circuit would still operate in the desired manner.

This effect is achieved by the series diodes shunting $R_1$. Since each diode has a junction voltage drop of about 0.8 volts at a few milliamps, the drop across $R_1$ must be 1.6 volts before the current will flow freely through the diode path.

One further major effect must be considered. The negative feedback loop through the three transistors is a possible source of oscillations.

The circuit was actually found to oscillate when the first model was tested. However, a new model, laid out as efficiently as possible, keeping leads short and with power supplies bypassed, was apparently free from oscillation.

A first order attempt was made to investigate the possibility of loop oscillation as follows: The loop was first studied to see at what frequency the phase shift attributed by individual transistors reached a total of 360 .

The loop gain was checked to see if it is greater than unity at this frequency. For this test $T_1$ and $T_2$ were SM1530's and $T_3$ was an SM5334 transistor. These were picked because of their similar frequency characteristics. This choice tends to increase the possibility of oscillation.

The current gain of both $T_3$ and $T_1$ (each in grounded-base configuration for the purpose of this discussion) roll off at their alpha cutoff frequency while $T_2$ gain degenerates at its beta cutoff frequency because of its grounded emitter use.

Since the beta cutoff frequency is only one over beta as large as the alpha cutoff, the tendency for oscillations might be increased by a choice of $T_2$ with a higher beta cutoff. This is unrealistic, however, since in any real circuit, power considerations would force $T_1$ and $T_2$ to be of the same type.

The beta cutoff was found to be about 500 KC (see Figure 16) for both transistors. Midband gain for the SM1530 was found to be

140, while that of the SM5334 was 110.[3]

Since

$$f_\alpha = \beta f_\beta$$

the alpha cutoff for the SM1530 will be 70 megacycles and that of the SM5334 will be 55 megacycles.

The phase shift of a transistor is very nearly 90° at one decade above its three db point. Since the alpha cutoff of $T_1$ and $T_3$ are well above the plus one decade point for $T_2$ (by 5 megacycles), the phase shift in $T_2$ can certainly be considered to be 90° (in addition to the current reversal in the base and the collector of $T_2$).

This means that the necessary phase shift for oscillations will come at approximately the three db point of $T_1$ and $T_3$ where a total of 90° phase shift will have to be contributed by the pair. This frequency is found in Figure 14 to be 60 megacycles.

Input impedance at this frequency was not measured, but it can be seen from Figure 15 that it will be very low.

To calculate the gain around the circuit, it is "broken" at some point. If, for instance, this is done at "A", a small oscillation trying to develop will split between $R_1$ and the impedance looking into the emitter of $T_3$ which is

$$Z_E = \frac{1}{\beta}\left(Z_{in} + 1000 /\!/ 100\right)$$

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[3]For a discussion of methods of measurements of high frequency parameters see J. F. Cleary, G. E. Transistor Manual (General Electric Co., Syracuse, New York), 1964.

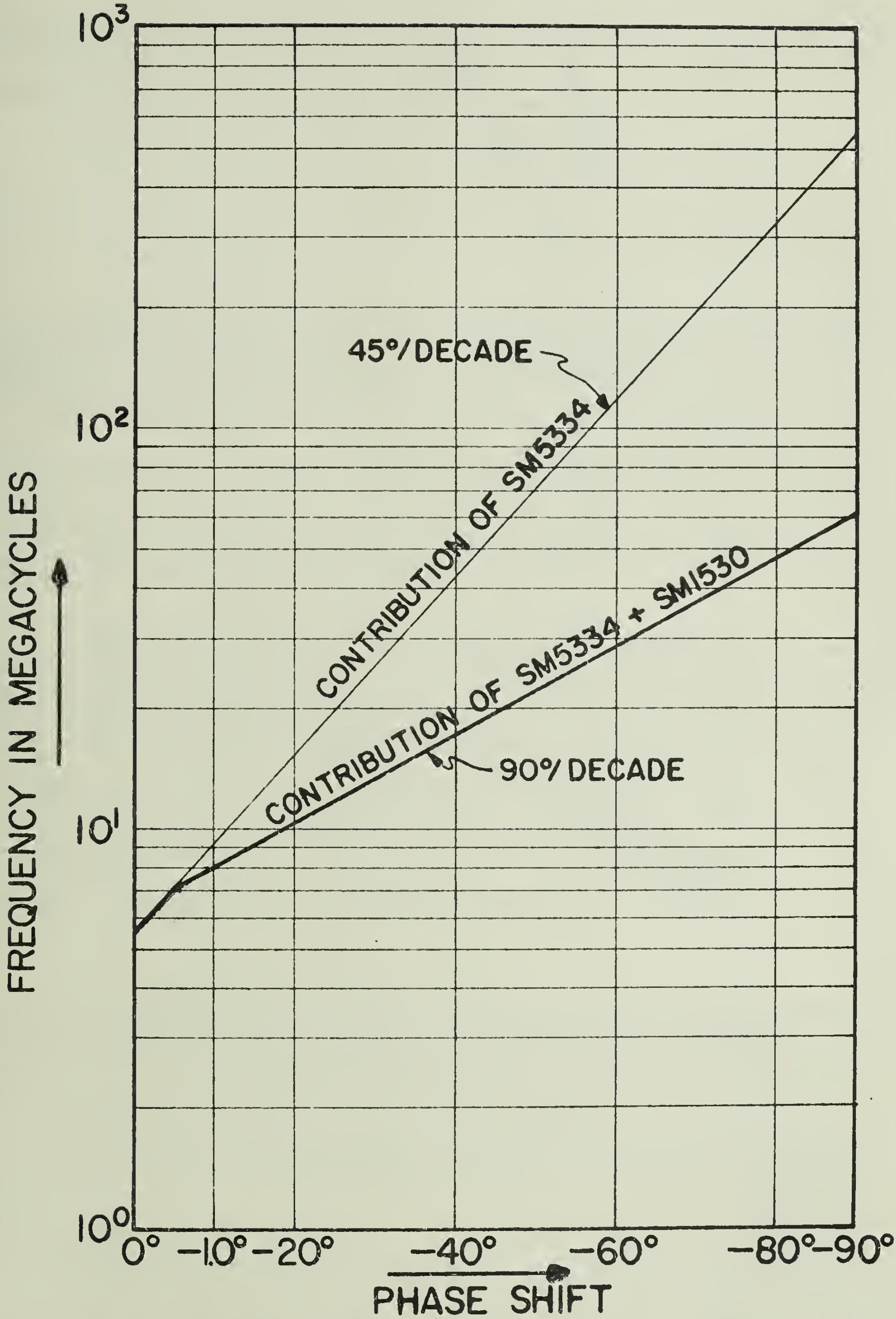


FIGURE 14. PHASE SHIFT IN THE COMMON BASE TRANSISTOR CONNECTION OF $T_3 + T_1$ IN FIGURE 13.

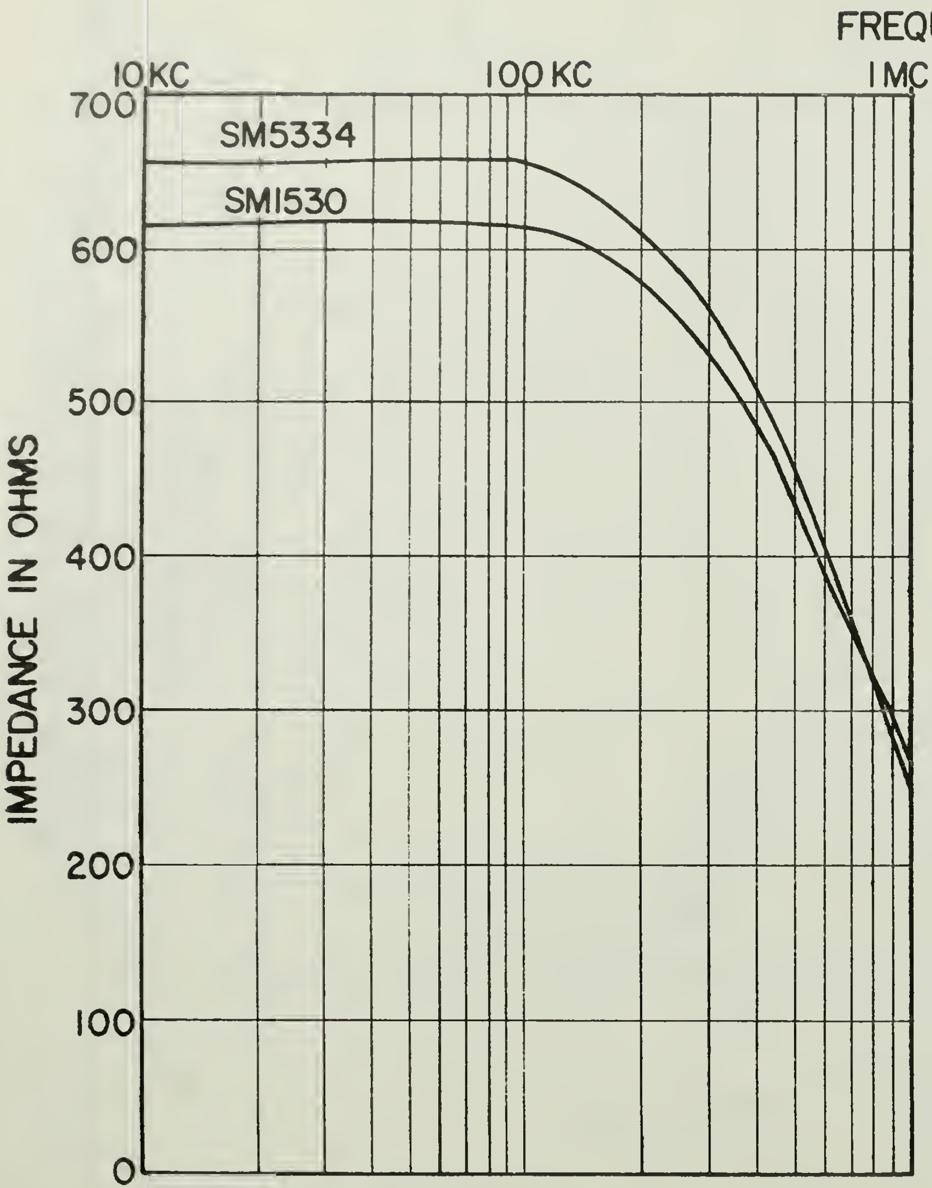


FIGURE 15. MEASURED INPUT IMPEDANCE VS FREQUENCY.

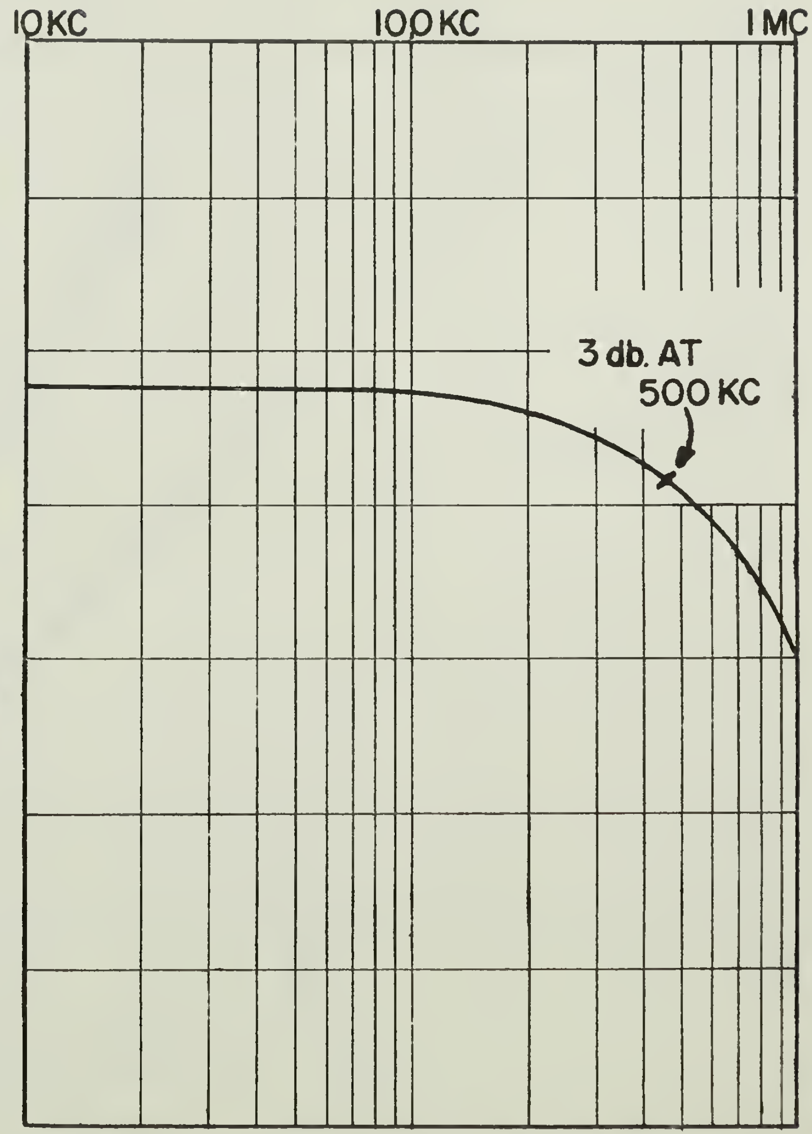


FIGURE 16. MEASURED COMMON EMITTER CURRENT BANDWIDTH OF THE SM1530 AND SM5334.

where $Z_{in}$ is the input impedance of the transistor in the common emitter configuration as was shown in Figure 15.

If this current splitting situation and transistor gain at 60 megacycles are considered around the entire loop, the loop gain is found to be somewhat greater than unity, creating the tendency to oscillate.

This tendency was observed experimentally when the input was driven with a fast rise input (pulse or a square wave).

One method that can be used to avoid these oscillations is to use a transistor for $T_3$ which is very high speed with respect to $T_1$ and $T_2$. This staggers the corner frequencies, making the loop gain lower at the 180 degree phase shift frequency.

Another method is to observe that the phase shift in the loop is due to the transistors appearing as R-C equivalent circuits, causing a lag in the current around the loop. An artificial lead time can be introduced by inserting a capacitor of 10 to 100 pf across the collector and emitter of $T_3$. This also has the desirable characteristic of reducing the rise time of the circuit output by a factor of two or three.

The loading that an output stage places upon its driver is very important. This circuit was found to have the very desirable low loading characteristics shown in Figure 17. Figure 18 shows that the output voltage lags the input voltage by a very small amount even for large loads.

The circuit of Figure 13 does then have the properties being sought for a high current drive output stage.

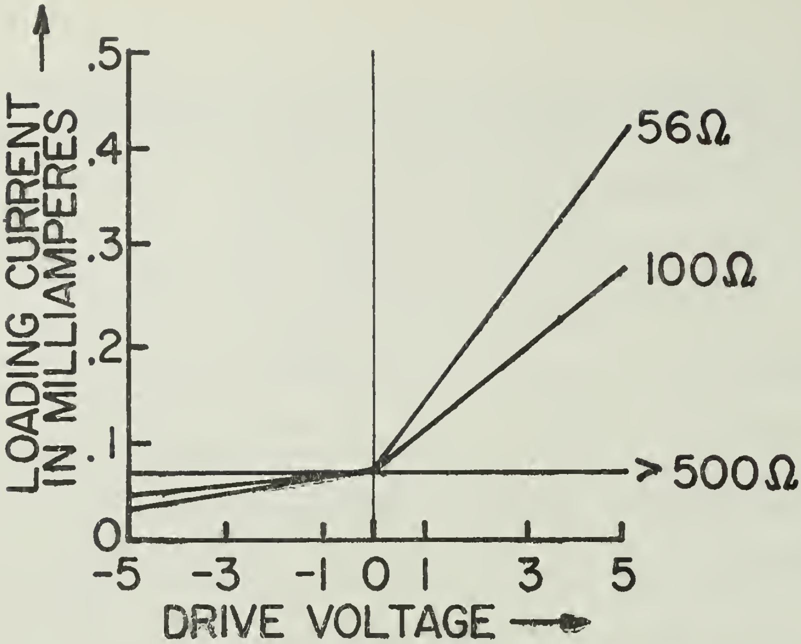


FIGURE 17. LOADING OF A SIMULATED 1K PREAMPLIFIER STAGE AS A FUNCTION OF LOAD RESISTANCE AND DRIVE VOLTAGE. (POWER SUPPLIES OF #10 USED.)

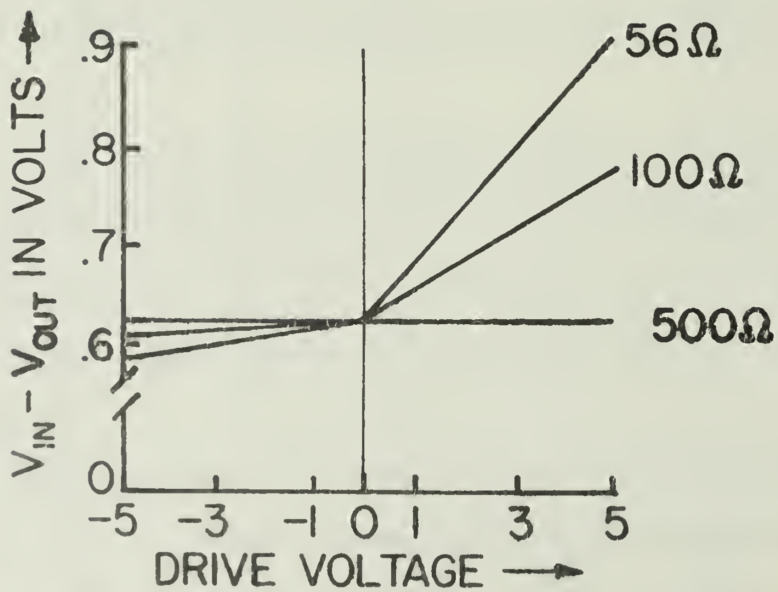


FIGURE 18. OUTPUT LAG VOLTAGE AS A FUNCTION OF LOAD RESISTANCE AND DRIVE VOLTAGE.

If the properties of the circuit in Figure 7 could now be combined with those of Figure 13, an amplifier having the properties of Figure 1 would result. An attempt at this goal is described in the next section. At the present the amplifier output stage discussed in this section is the most appropriate yet found as an answer to the general problem originally posed.

## 6. HIGH VOLTAGE-HIGH CURRENT DRIVE

In the attempt to combine the two capabilities of high current and high voltage drive, the circuit in Figure 19 was considered.

This circuit does have some of the properties that were being sought; that is, the capability of either high voltage swings or alternately high current drive at lower voltages, depending on the size of the load.

The transistor $T_1$ has relatively high current capabilities while $T_2$ has high voltage potential. The diode isolates the positive 100 supply from the low-voltage transistor $T_1$. $T_3$ provides voltage amplification and drives the base of $T_2$.

A large load will tend to isolate the positive 100 volt supply and 10K resistor, allowing $T_1$ the major role. $T_1$ does not have any voltage amplification, but is adaptive to large loads.

For small loads, $T_2$ with its collector resistance will provide additional voltage amplification and permit large voltage swings.

This amplifier, however, does not allow both positive and negative swings and from that standpoint alone probably would not be a very useful device.

There is further the possibility of uncontrolled currents through the $T_1$, $T_2$ path, introducing the problems encountered earlier.

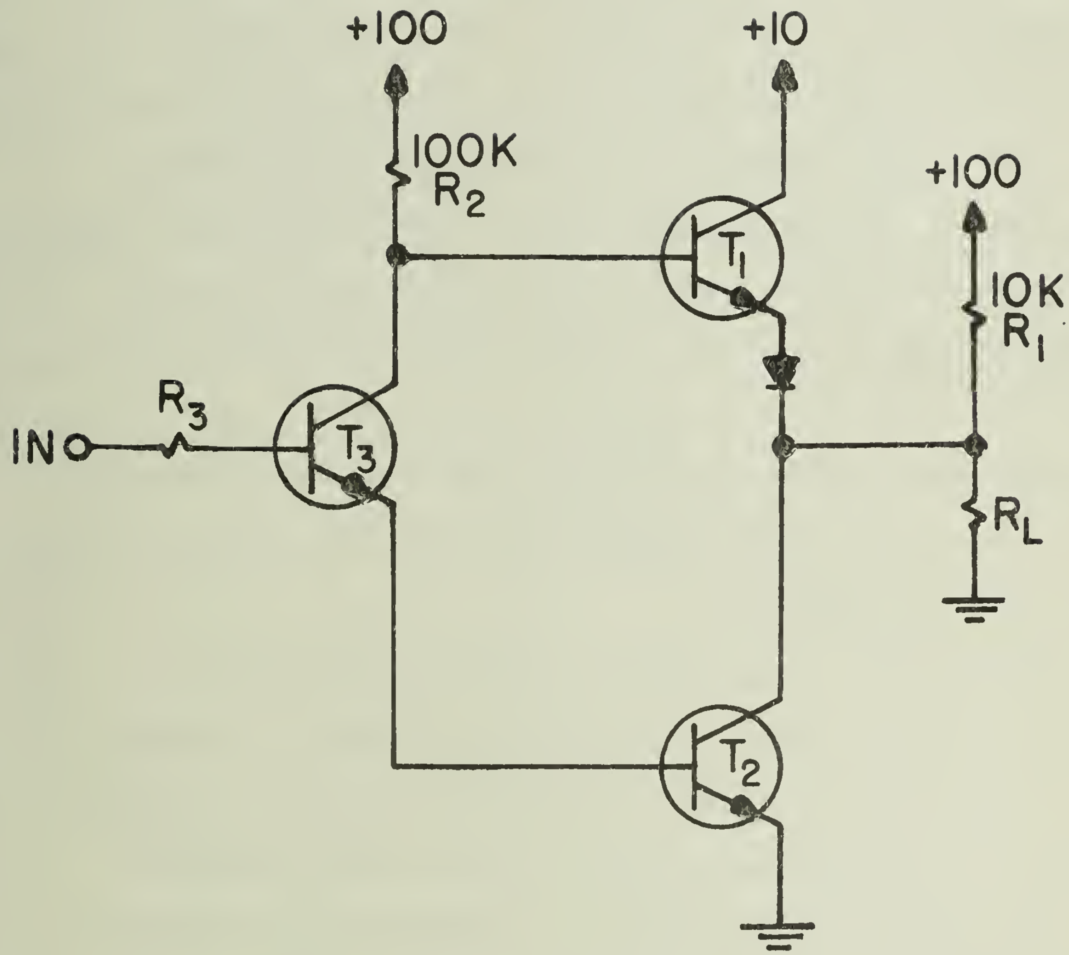


FIGURE 19. UNBALANCED OUTPUT STAGE USING BOTH HIGH VOLTAGE AND HIGH CURRENT DEVICES, APPROXIMATING ONE HALF THE OUTPUT CHARACTERISTICS OF FIGURE 1.

# CONCLUSION

The original goal has been the generation of an amplifier with output characteristics as shown in Figure 1; that is, of providing capabilities of high current, high voltage drive, though not simultaneously.

For the driver stage, a differential amplifier was chosen because of its low drift properties. A driver stage of the same type was considered, but was not used because of its inherent current driving inefficiency produced by the split of total supply current between the load and the active element.

This particular problem of circuit effectiveness was surmounted by use of complimentary emitter follower circuits and the coupling circuits between $T_1$ and $T_2$ of Figure 13.

Although there was an apparent solution in the circuit of Figure 7 and a partial solution in the circuit of Figure 19, the push-push, or pull-pull nature of these configurations introduced the problem of deadband, or alternately, uncontrolled currents between supplies.

The original problem seems now to be modified and to have removed itself then from the design of configurations with the desired properties of Figure 1 to the design of a configuration controlling dead band and uncontrolled current flow.

As was discovered, attempts to control dead band seem to increase the possibility of uncontrolled currents, and preventing the short circuit possibility seems conversely to insert dead band.

A final solution appears to lie in an attempt to stay in between these two states. When this was tried in the circuit of Figure 11, the

problem of instability was introduced.

Possibly this might be controlled in the circuit of Figure 11 by an investigation of the effects of the base biasing resistors on the rest of the circuit in the various conducting states and by a reduction of the positive feedback introduced by the control transistors.

In the search the possibly unique circuit of Figure 13 was discovered. The circuit had the extremely useful property of being able to drive small loads efficiently within a limited voltage range. This circuit could possibly be incorporated in a circuit in an attempt to achieve the output characteristics of Figure 1.

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